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10/569,825	02/01/2007	Marcel Lapointe	OBL-007-US	5375

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EXAMINER	
HUANG, DAVID S	
ART UNIT	PAPER NUMBER
2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/569,825	LAPOINTE, MARCEL	
	Examiner	Art Unit	
	DAVID HUANG	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,9,10,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12 and 13* is/are rejected.

7)☒ Claim(s) *4-6,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 12 and 13 is withdrawn in view of the newly discovered reference(s) to Mizoguchi et al. (US 5,005,185) and Shusterman et al. (US 6,590,933). Rejections based on the newly cited reference(s) follow.

Claim Objections

2. Claims 4-6, 9, 10, 12 and 13 are objected to because of the following informalities:

Claim 4 recites "Q latch means" and "Q multiplexer/multiplier means" and "Q inputs." However, the notation Q for the same number of latches, mux/muls, and inputs, is confusing, and may be construed to mean "quadrature". It is suggested to applicant to define Q (for example, as an integer greater than 1), to improve the clarify of the claims.

Claims 5, 6, 9 and 10 are dependent on claim 4, and are also objected.

Claims 12 and 13 similarly use Q, and are also objected.

Claim 12 also recites "the reference clock rate" on line 7, but should be "a reference clock rate".

Claim 13 recites "the clock rate" in line 6, but should be "a clock rate".

Claim 13, line 8, recites "summing network_for" but the underscore should be removed.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizoguchi et al. (US 5,005,185) in view of Shusterman et al. (US 6,590,933).

Regarding claim 12, Mizoguchi et al. discloses a method for providing a feed forward equalizer (FFE) in a transversal finite impulse response (FIR) filter for transmitting data bits that are shifted through delay elements, and each delay element being coupled to a corresponding multiplier and all of the multiplied outputs are summed, the method comprising:

i) supplying the data bits to be processed to Q shift registers (transversal filters 2 and 4, Fig. 1, col. 3, lines 1-17) operating at a shift rate that is the quotient of the reference clock rate divided by Q (half the rate of the clock pulse, col. 3, lines 10-13; data streams decomposed into N (2 or more) sequences, and operate at clock signal divided by N, col. 1, line 66 - col. 2, line 7, Figs. 1 and 2; clock recovery 48 and divide by two frequency divider 9, both in Fig. 1, see also col. 4, lines 44-57).

However, Mizoguchi et al. fails to expressly disclose ii) multiplexing said Q shift registers to a FIR FFE multiplier summing network for a unit interval period defined by said reference clock rate such that each shift register of said Q shift registers is successively multiplexed to the FIR FFE multiplier summing network in successive unit interval periods.

Nevertheless, Mizoguchi et al. discloses an adaptive transversal equalizer with a transversal filter multiplier summing network following latch 34, including multipliers 35 and summer 36 (Fig. 2). In transversal filter 2, the output of summer 36 is sent to in-phase channel adder 10 which is connected to the first input of mux 14. In transversal filter 4, which receives

the input signal after a 1-symbol delay (DL 3, Fig. 1), the corresponding output 4(1) is sent to in-phase adder 11, which is connected to the second input of mux 14 (Figs. 1 and 2). Mux 14 also receives half rate clock fc/2 and full rate clock fc (Fig. 1). Mux 14 is supplied with the lower-frequency clock in order to receive output signals from the associated adders, and is supplied with the higher frequency clock to combine them into a single bit stream. Therefore, Mizoguchi et al. discloses applying the summing network first, then multiplexing the result of the summing network for successive unit intervals according to the high frequency clock fc.

Thus, Mizoguchi et al. disclose everything claimed except for that the shift register outputs are multiplexed to the summing network. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to reverse the order of multiplexing and summing network, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

However, Mizoguchi et al. still fails to expressly disclose that the summing network is and FIR FFE multiplier summing network.

Shusterman et al. discloses a conventional decision feedback equalizer including an adaptive feed forward equalizer (FFE 105, col. 3, lines 58-60, Fig. 1a).

Because both Mizoguchi et al. and Shusterman et al. disclose adaptive equalizers, it would have been obvious to one of ordinary skill in the art to substitute one adaptive equalizer for the other for the predictable result of implementing an adaptive feed forward equalizer with a summing network.

Regarding claim 13, Mizoguchi et al. discloses a method for providing a decision feedback equalizer (DFE) in a transversal finite impulse response (FIR) filter for recovering data bits in a received data signal having a data rate defining a unit interval period comprising:

i) conditioning the received data signal (RX signal input 50, conditioned by LPF 45 and A/D converter 1, Fig. 1), and

ii) supplying the conditioned data signal to Q shift registers (transversal filters 2 and 4, Fig. 1, col. 3, lines 1-17), all said shift registers operating at a shift rate that is the quotient of the reference clock rate of the received data signal divided by Q (half the rate of the clock pulse, col. 3, lines 10-13; data streams decomposed into N (2 or more) sequences, and operate at clock signal divided by N, col. 1, line 66 - col. 2, line 7, Figs. 1 and 2; clock recovery 48 and divide by two frequency divider 9, both in Fig. 1, see also col. 4, lines 44-57).

However, Mizoguchi et al. fails to expressly disclose ii) multiplexing said Q shift registers to a FIR DFE multiplier summing network for a unit interval period defined by said clock rate of the received data signal such that each shift register of said Q shift registers is successively multiplexed to the FIR DFE multiplier summing network in successive unit interval periods.

Nevertheless, Mizoguchi et al. discloses an adaptive transversal equalizer with a transversal filter multiplier summing network following latch 34, including multipliers 35 and summer 36 (Fig. 2). In transversal filter 2, the output of summer 36 is sent to in-phase channel adder 10 which is connected to the first input of mux 14. In transversal filter 4, which receives the input signal after a 1-symbol delay (DL 3, Fig. 1), the corresponding output 4(1) is sent to in-phase adder 11, which is connected to the second input of mux 14 (Figs. 1 and 2). Mux 14 also

receives half rate clock fc/2 and full rate clock fc (Fig. 1). Mux 14 is supplied with the lower-frequency clock in order to receive output signals from the associated adders, and is supplied with the higher frequency clock to combine them into a single bit stream. Therefore, Mizoguchi et al. discloses applying the summing network first, then multiplexing the result of the summing network for successive unit intervals according to the high frequency clock fc.

Thus, Mizoguchi et al. disclose everything claimed except for that the shift register outputs are multiplexed to the summing network. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to reverse the order of multiplexing and summing network, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

However, Mizoguchi et al. still fails to expressly disclose that the summing network is and FIR DFE multiplier summing network.

Shusterman et al. discloses a conventional decision feedback equalizer including an adaptive decision feedback equalizer (DFE 140, col. 4, lines 11, Fig. 1a).

Because both Mizoguchi et al. and Shusterman et al. disclose adaptive equalizers, it would have been obvious to one of ordinary skill in the art to substitute one adaptive equalizer for the other for the predictable result of implementing an adaptive feedback equalizer with a summing network.

Allowable Subject Matter

5. Claims 4-6, 9 and 10 are objected to but would be allowable if rewritten to address the formal matters presented above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID HUANG whose telephone number is (571)270-1798. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSH/dsh
5/8/2010
/David Huang/
Examiner, Art Unit 2611

/CHIEH M FAN/

Supervisory Patent Examiner, Art Unit 2611